

# Active-HDL PDF Export

**version 7.2**

**Active-HDL™**  
Complete FPGA Verification Environment

**ALDEC**  
*The Design Verification Company*

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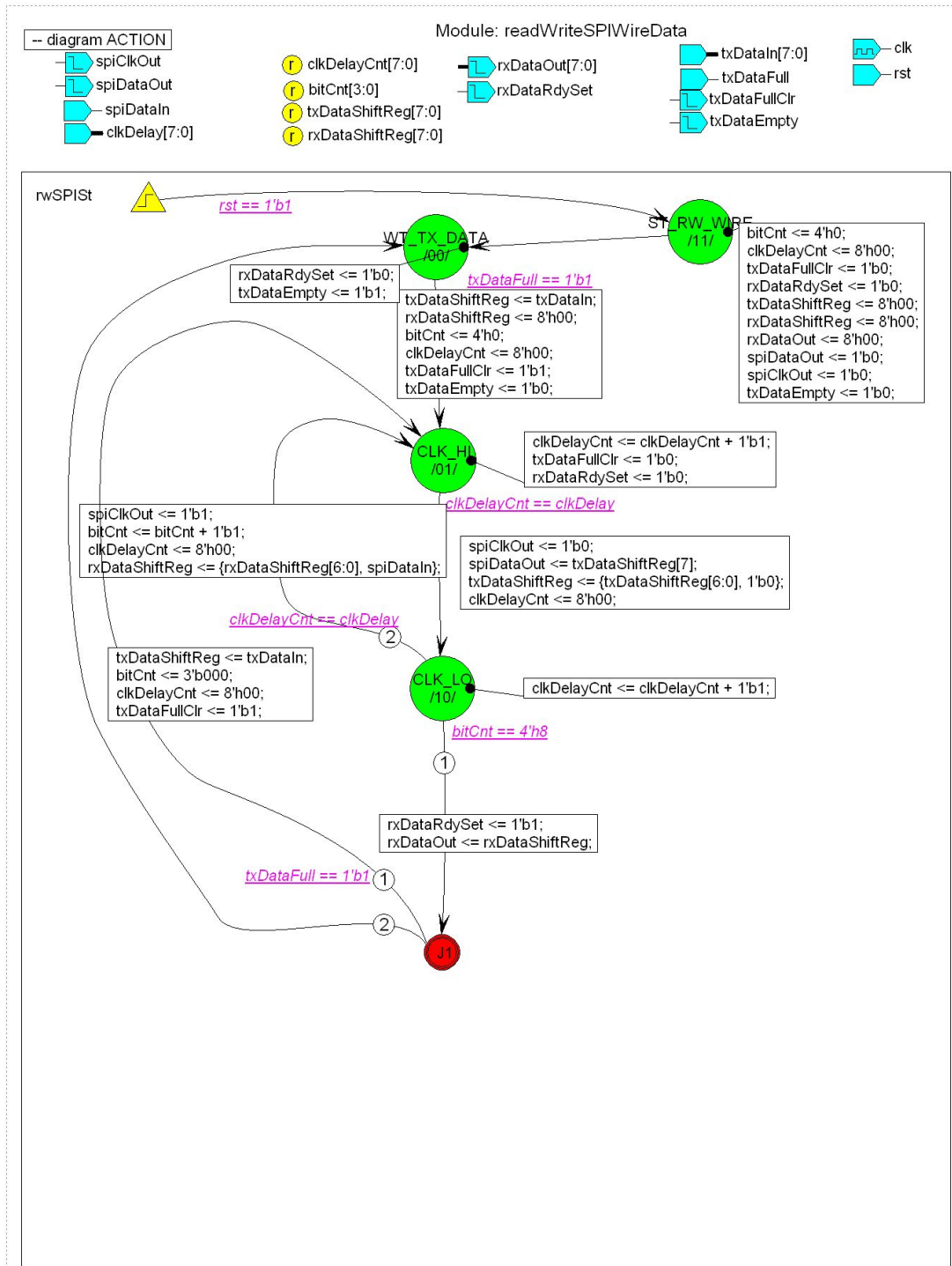
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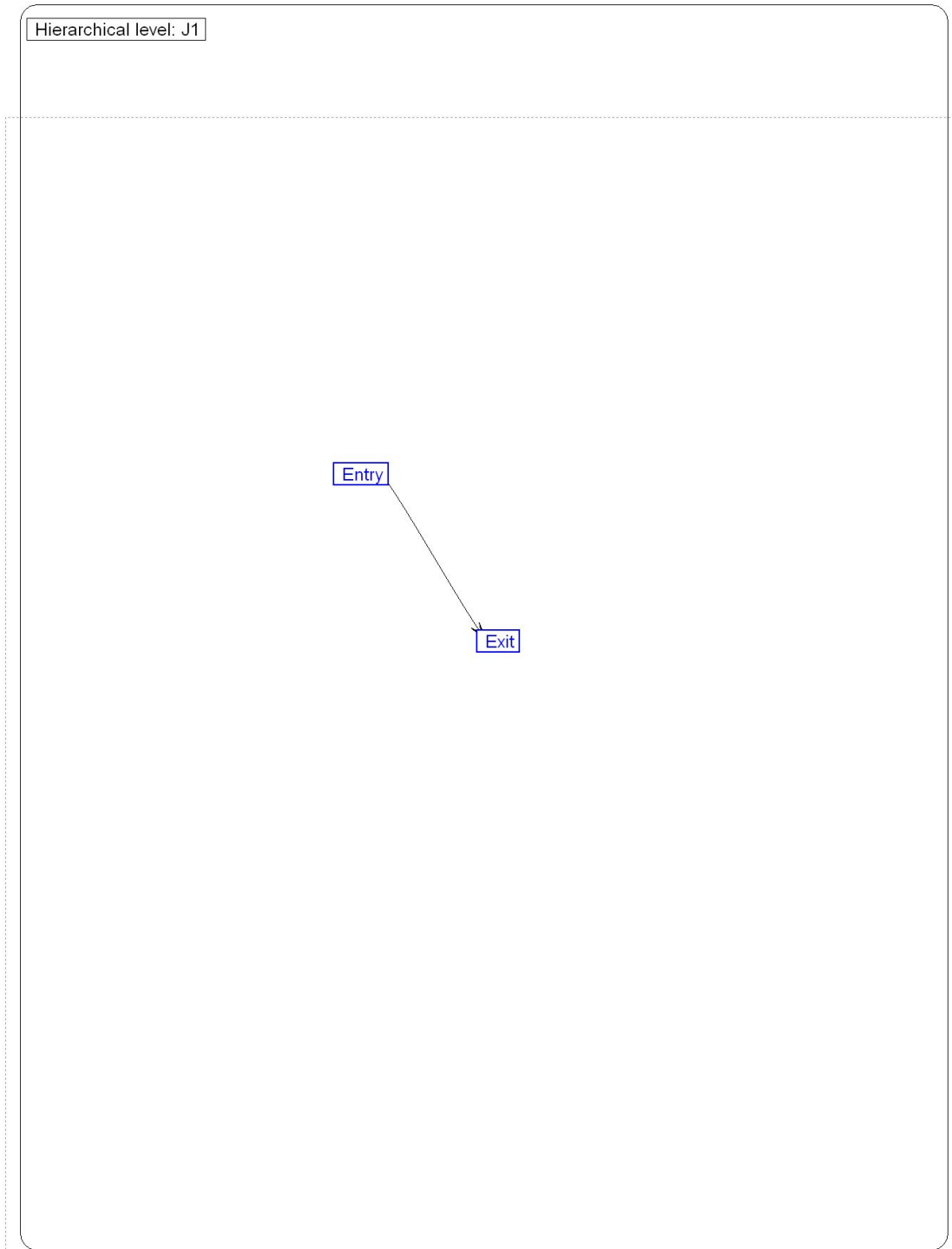
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## 2 design0

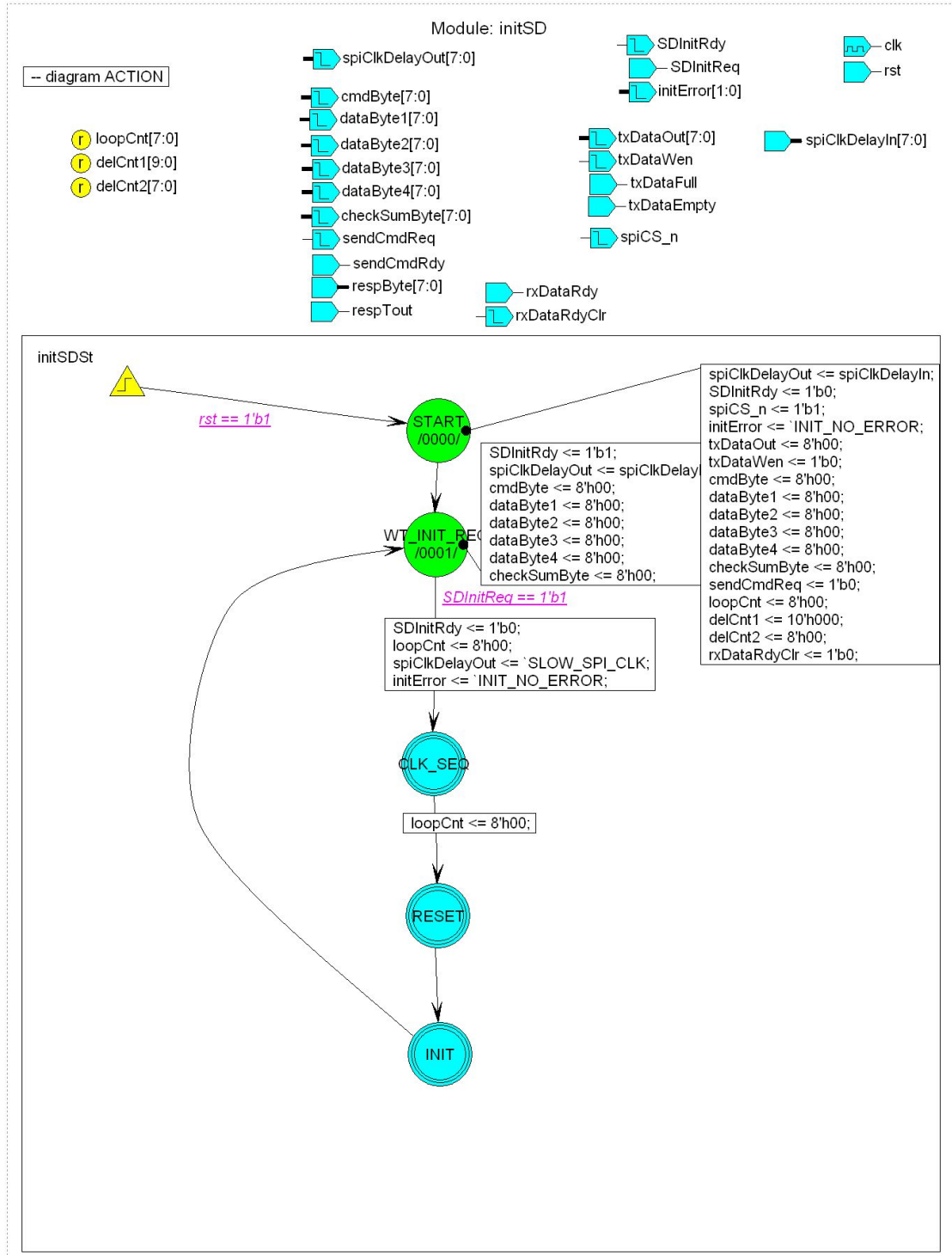
### 2.1 readWriteSPIWireData.asf



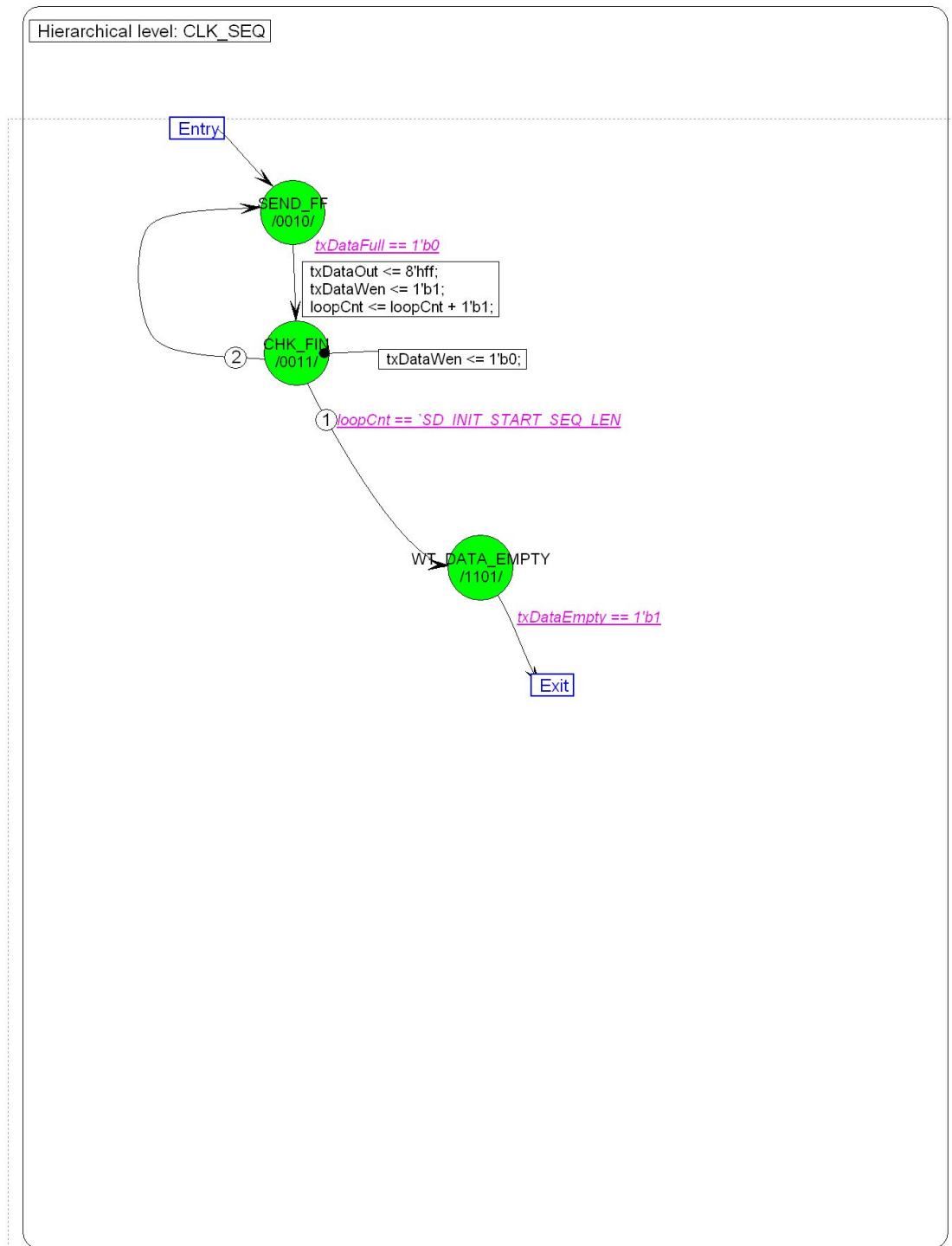
2.1.1 J1



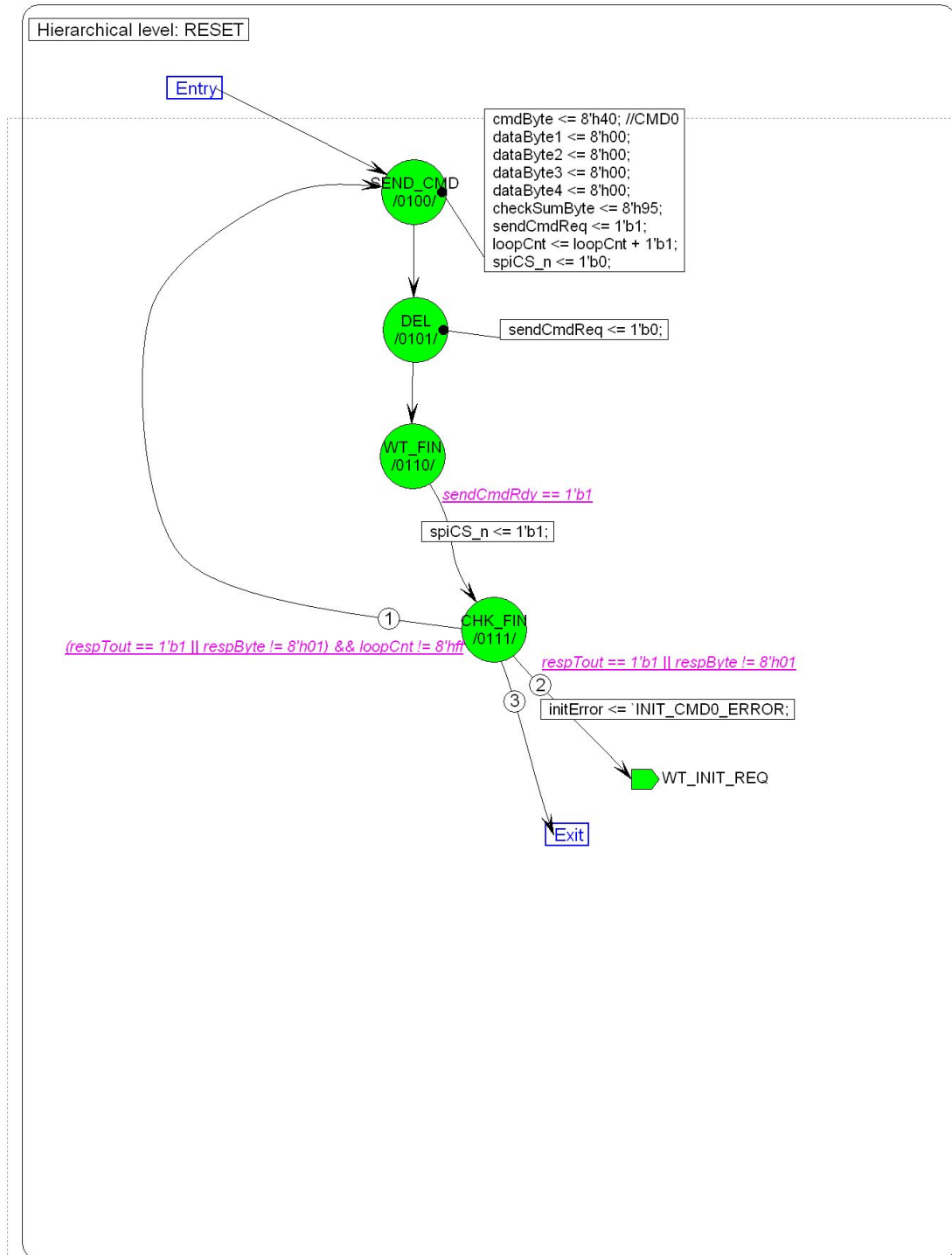
## 2.2 initSD.asf



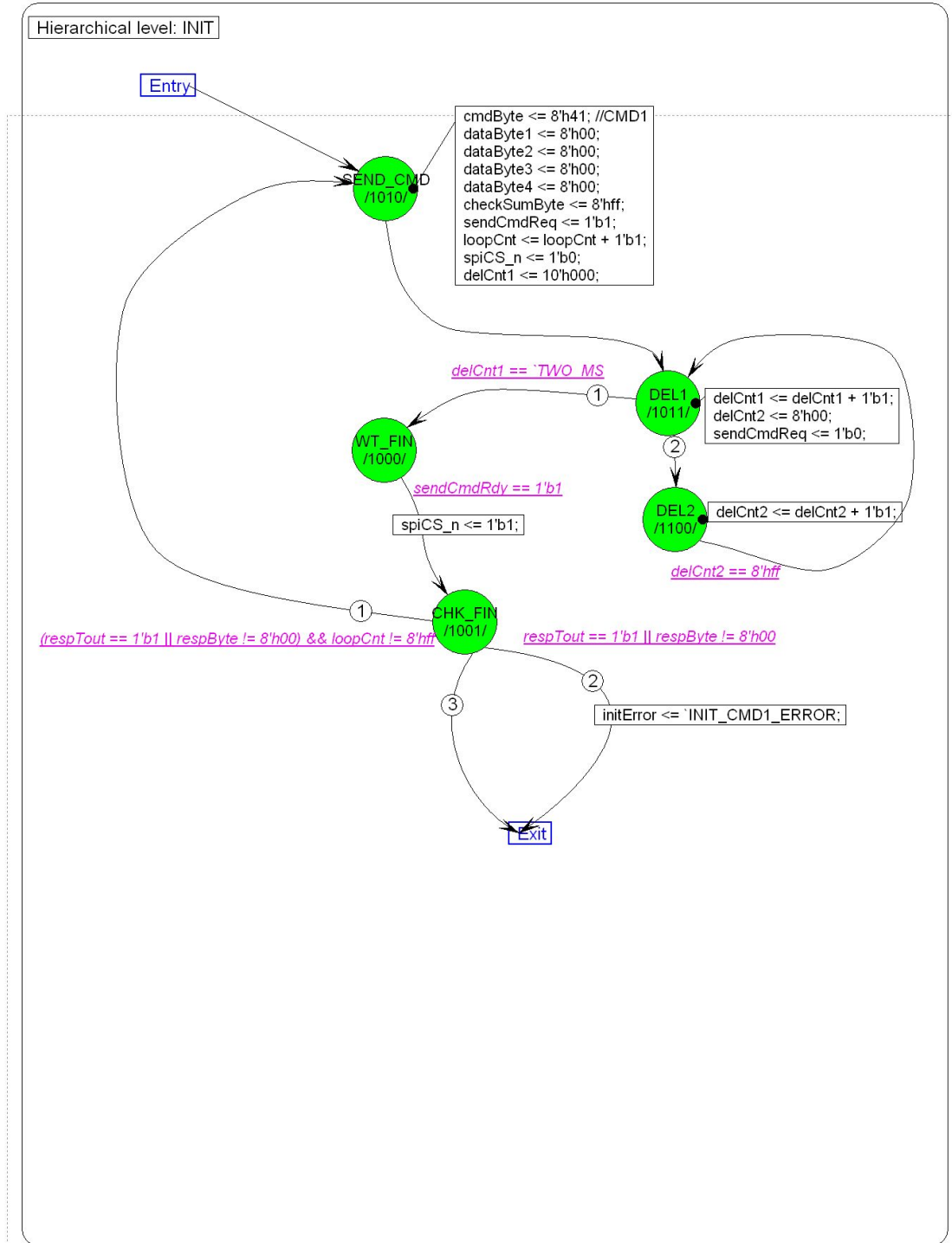
## 2.2.1 CLK\_SEQ



## 2.2.2 RESET

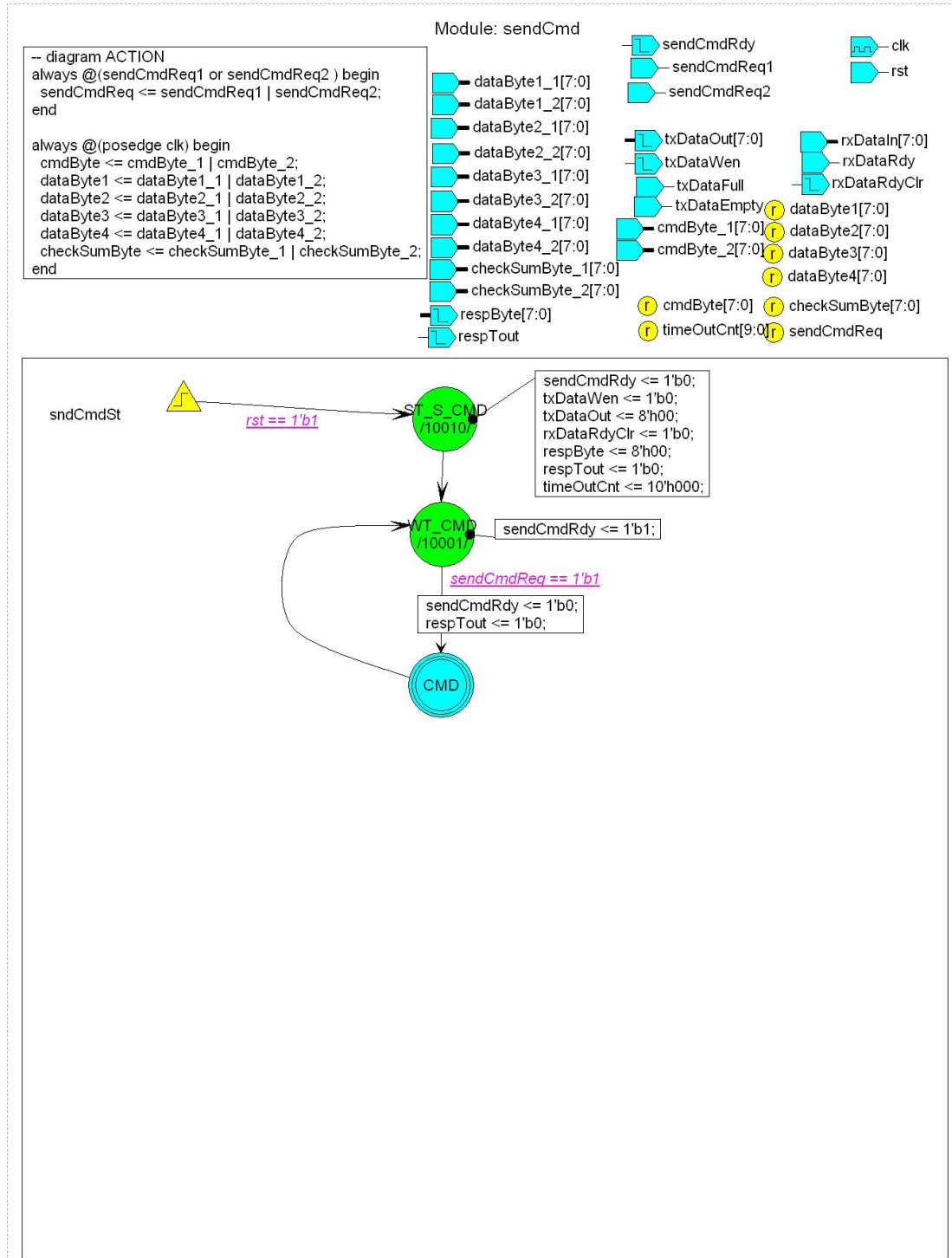


## 2.2.3 INIT

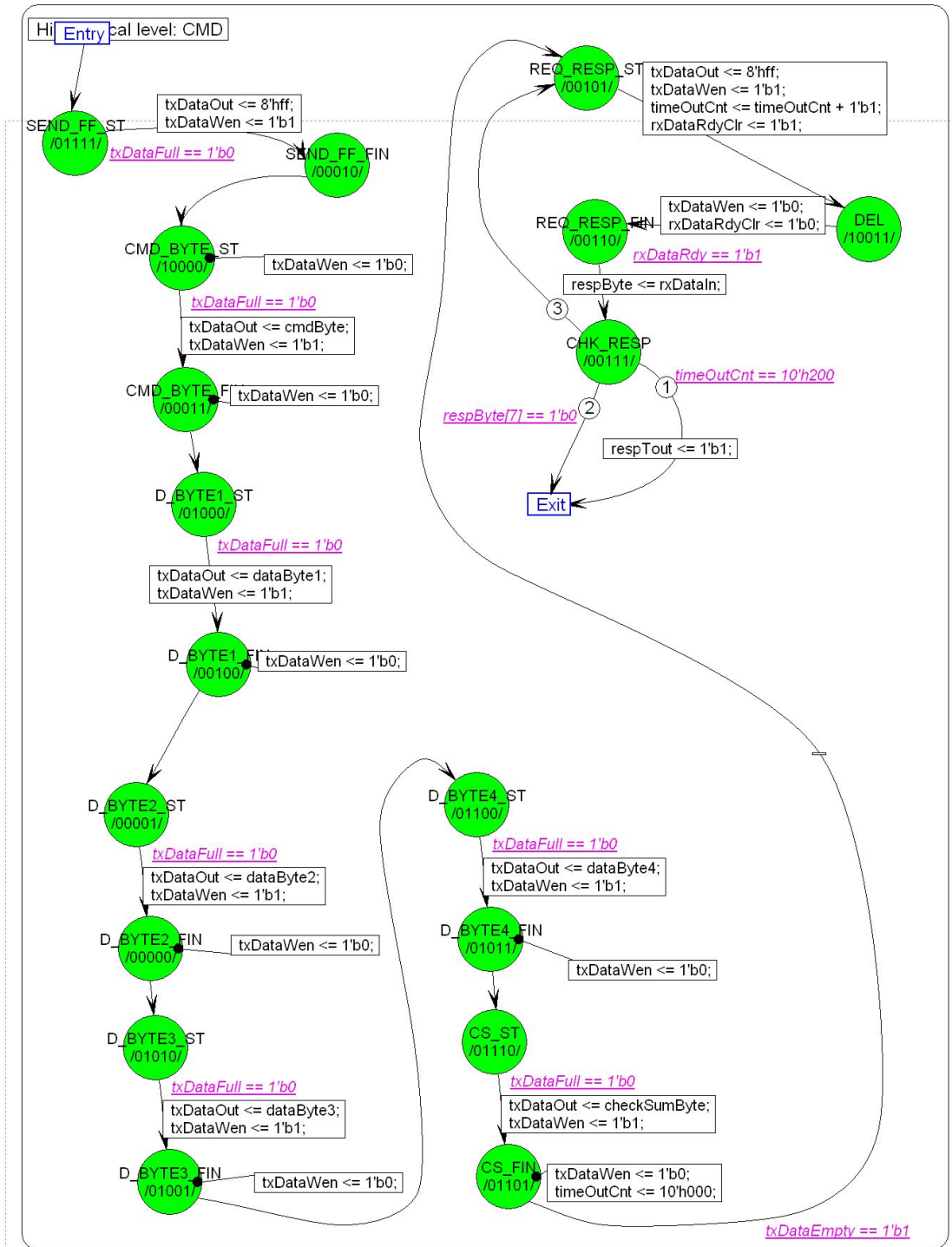




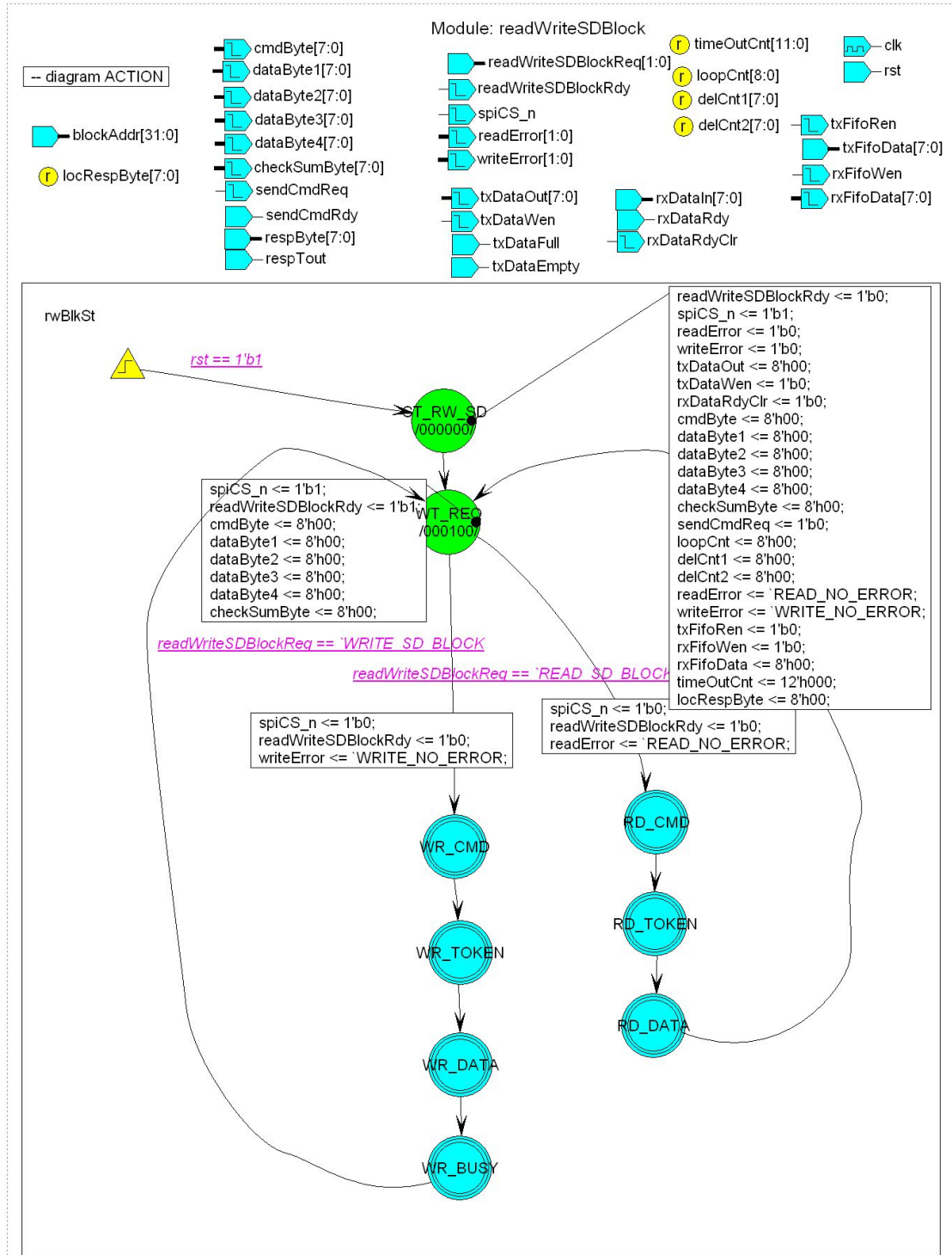
## 2.3 sendCmd.asf



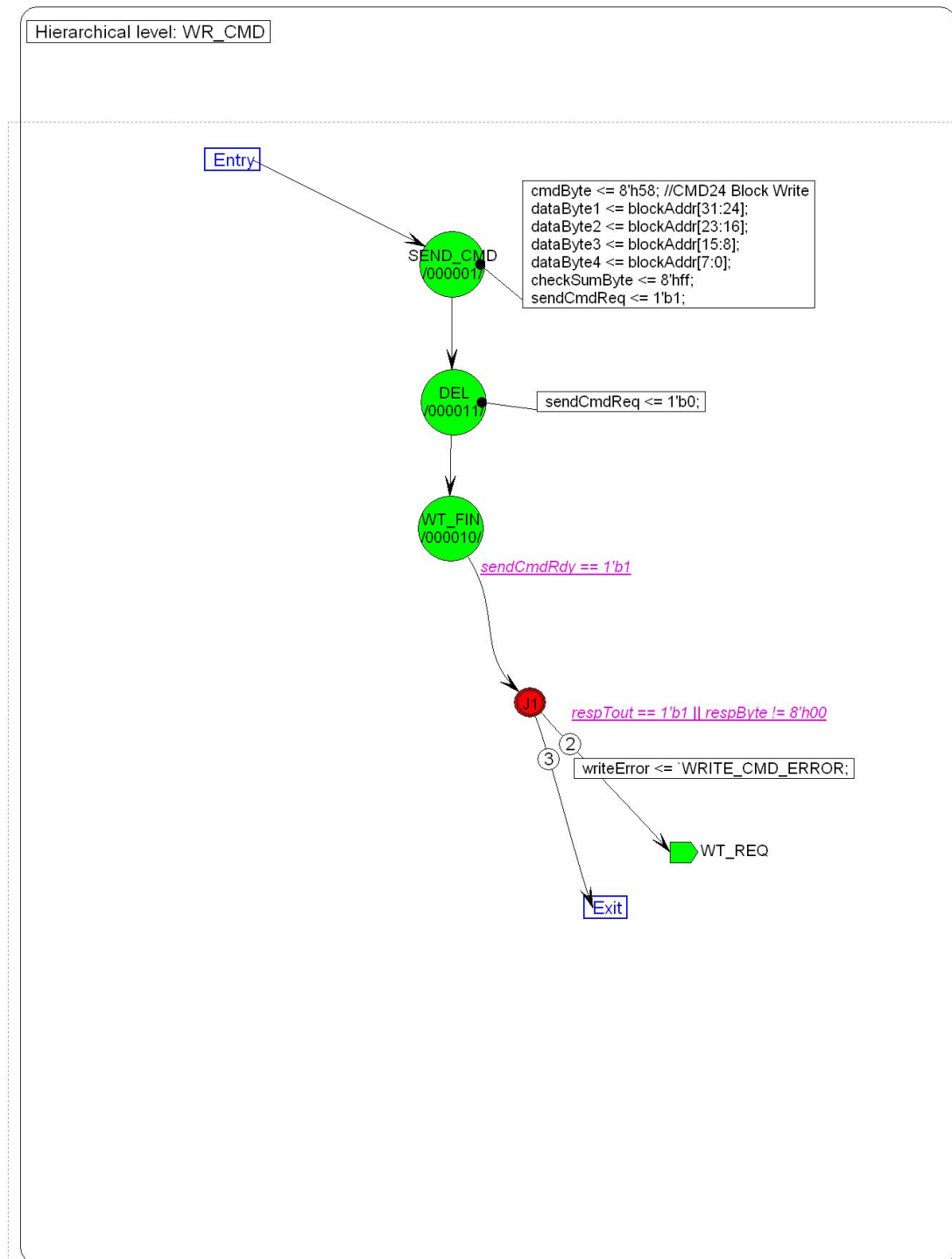
### 2.3.1 CMD



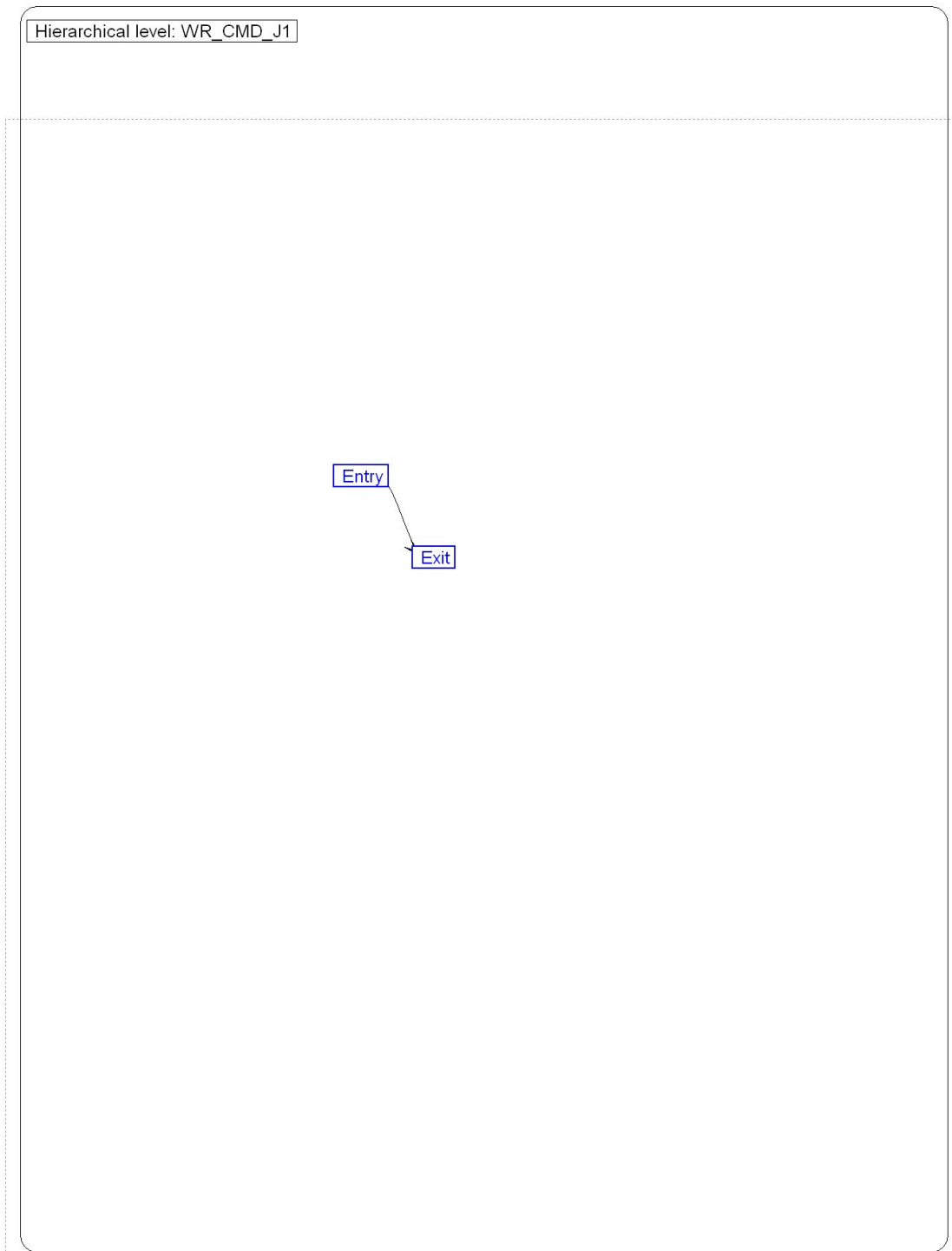
## 2.4 readWriteSDBlock.asf



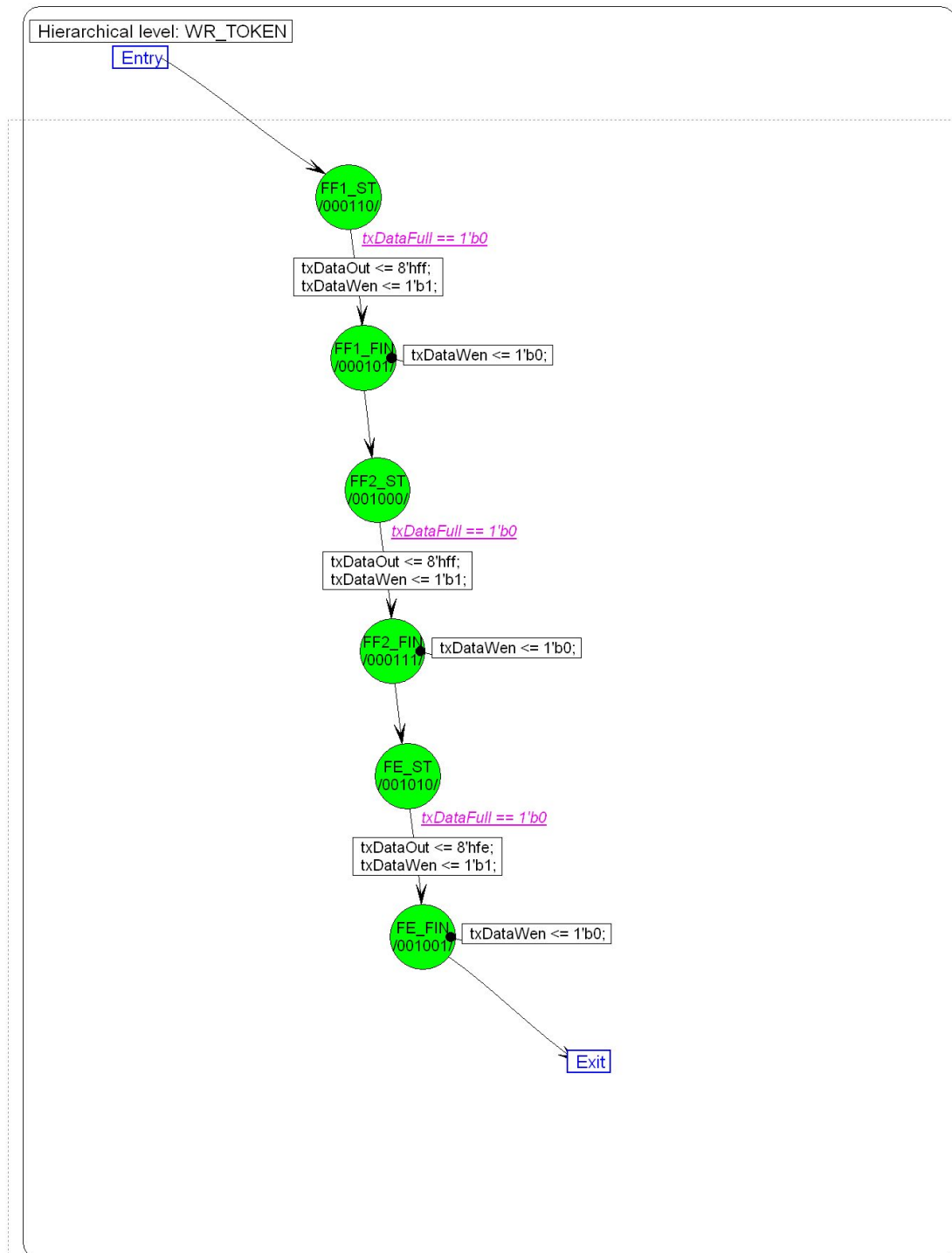
## 2.4.1 WR\_CMD



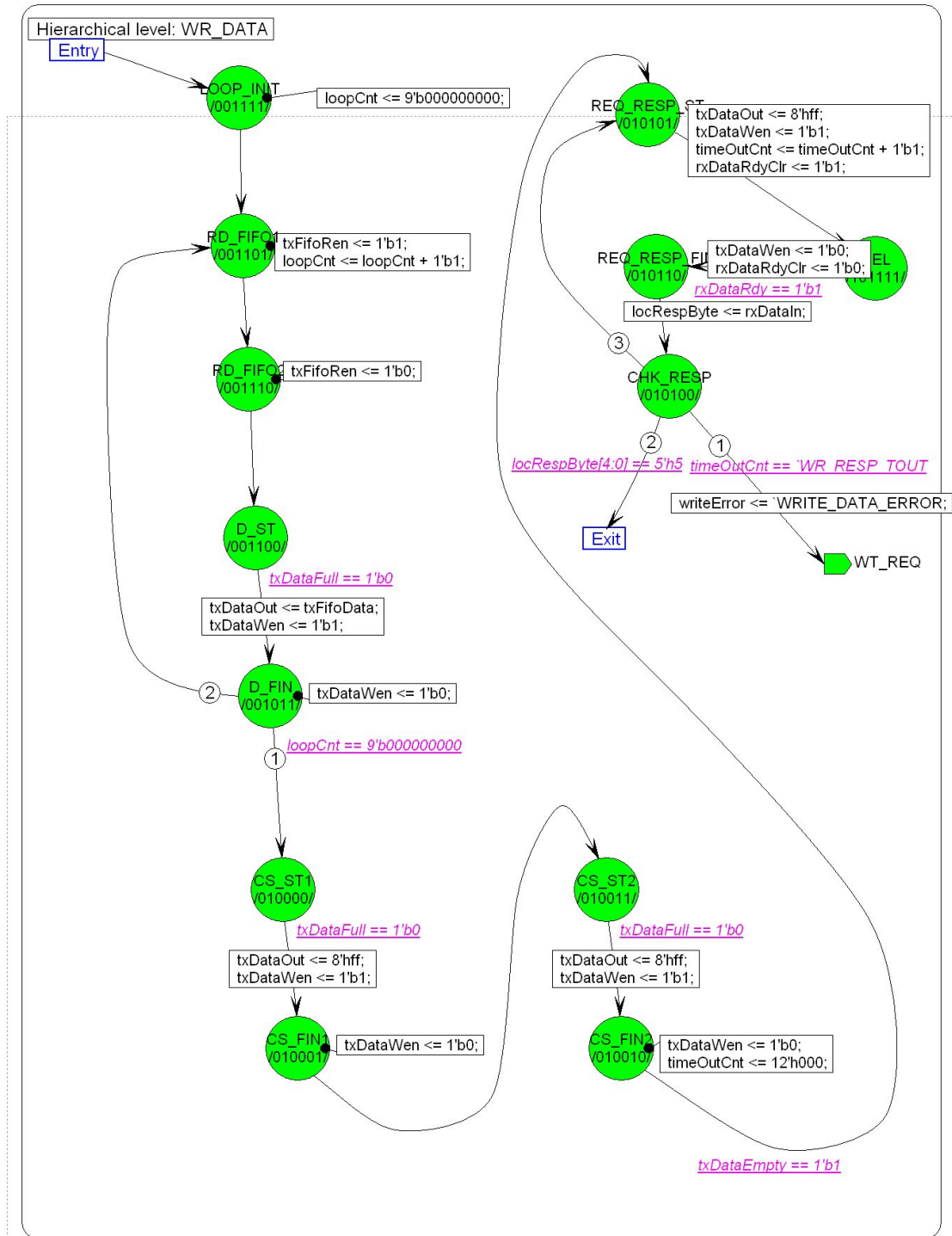
2.4.1.1 J1



## 2.4.2 WR\_TOKEN



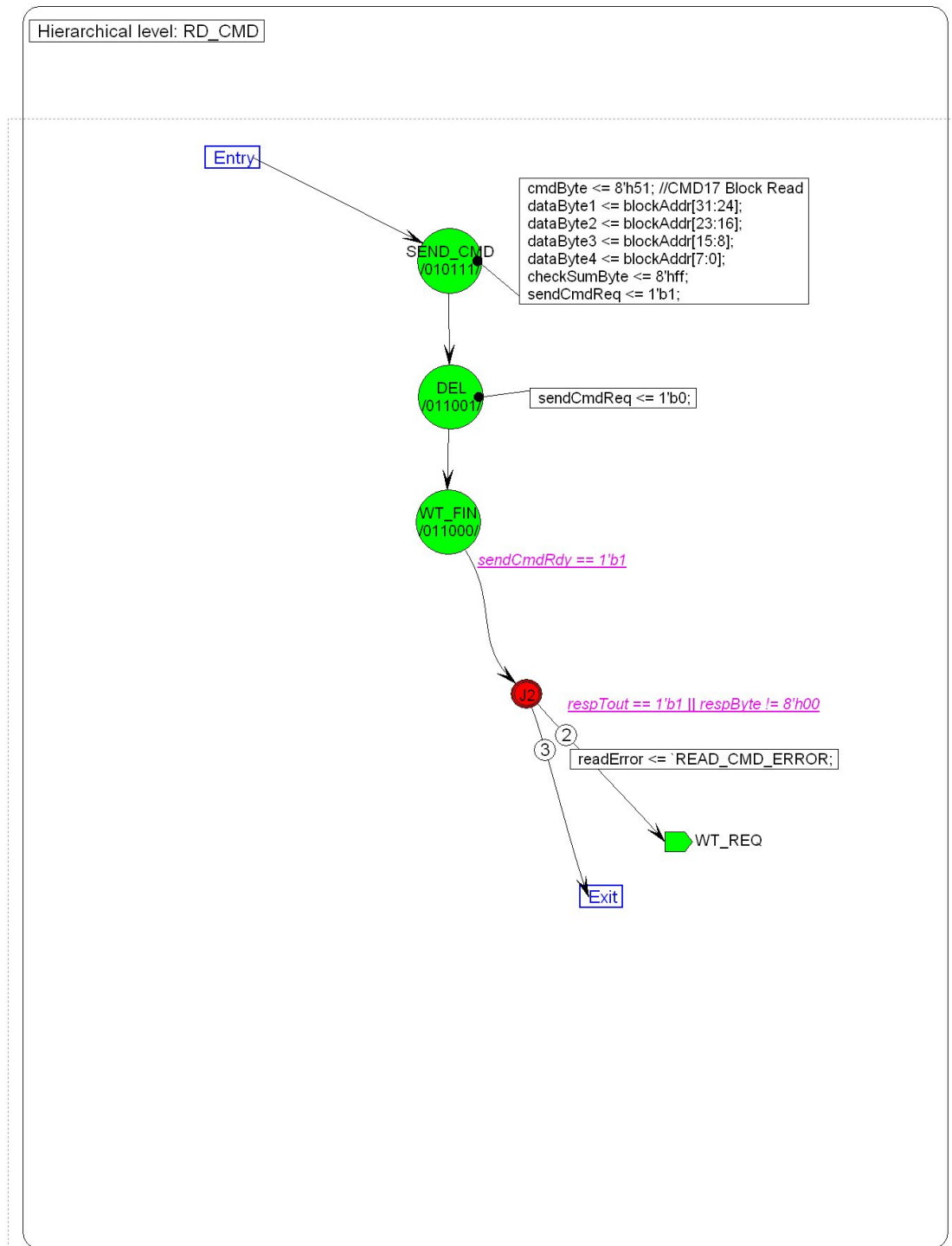
### 2.4.3 WR\_DATA



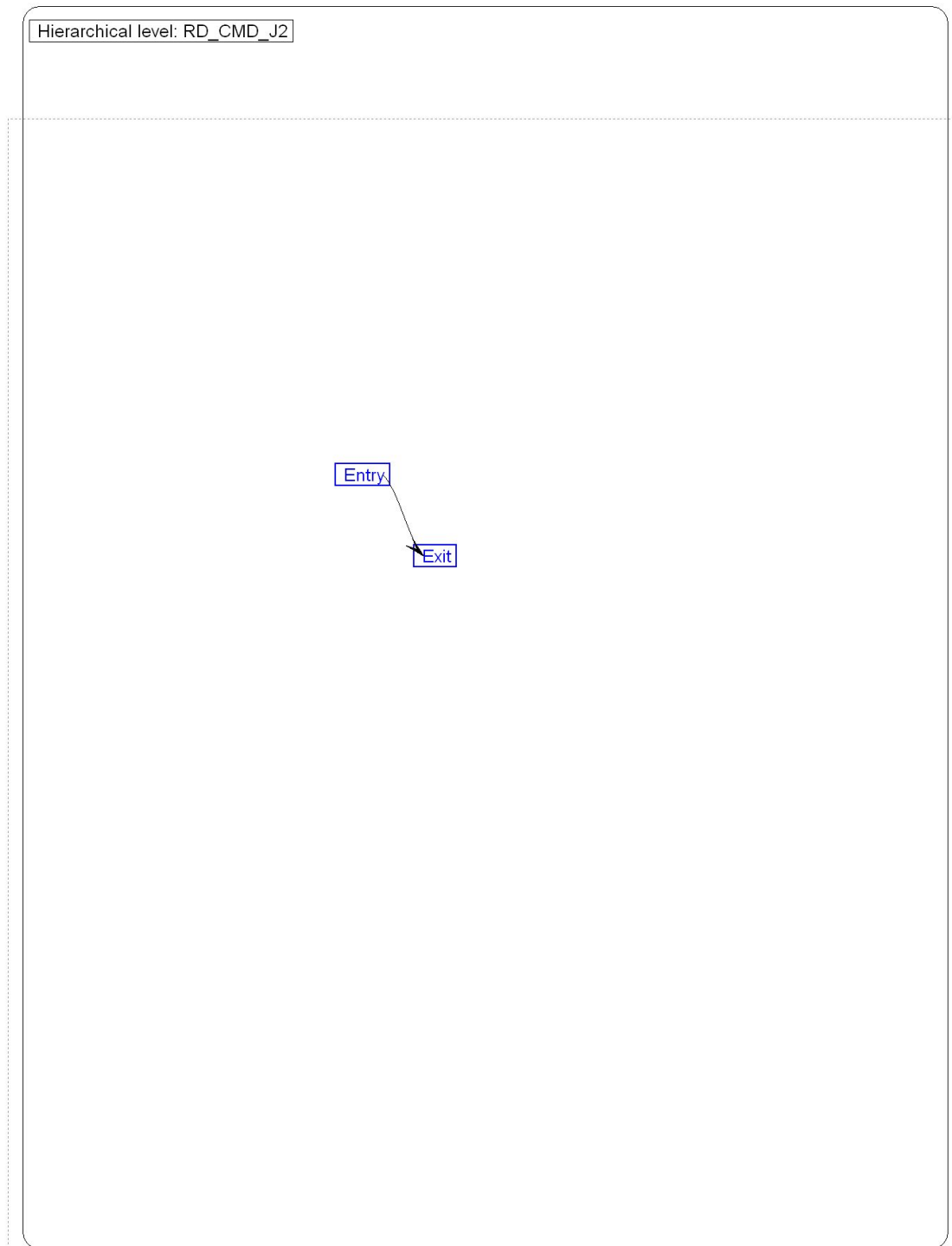




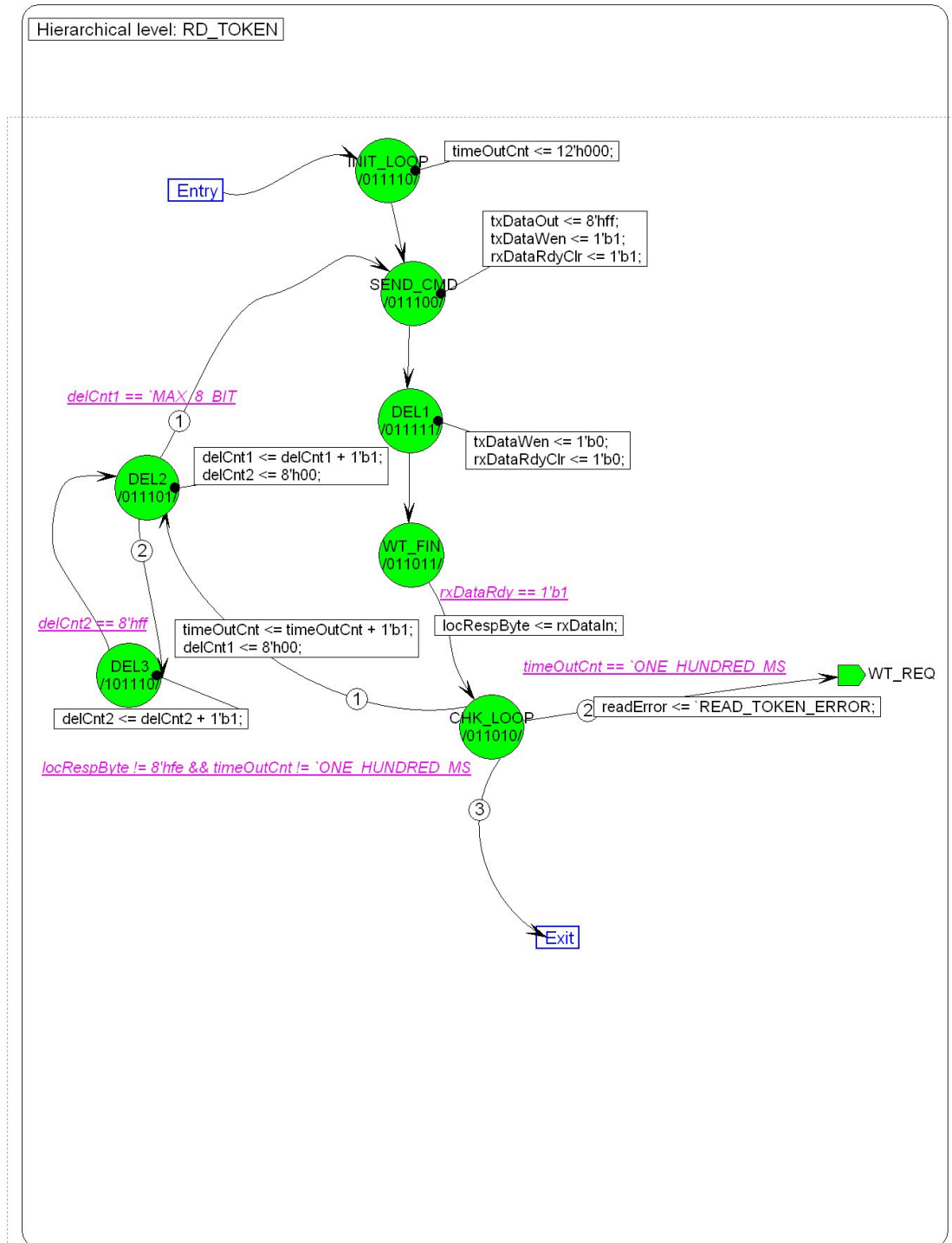
## 2.4.5 RD\_CMD



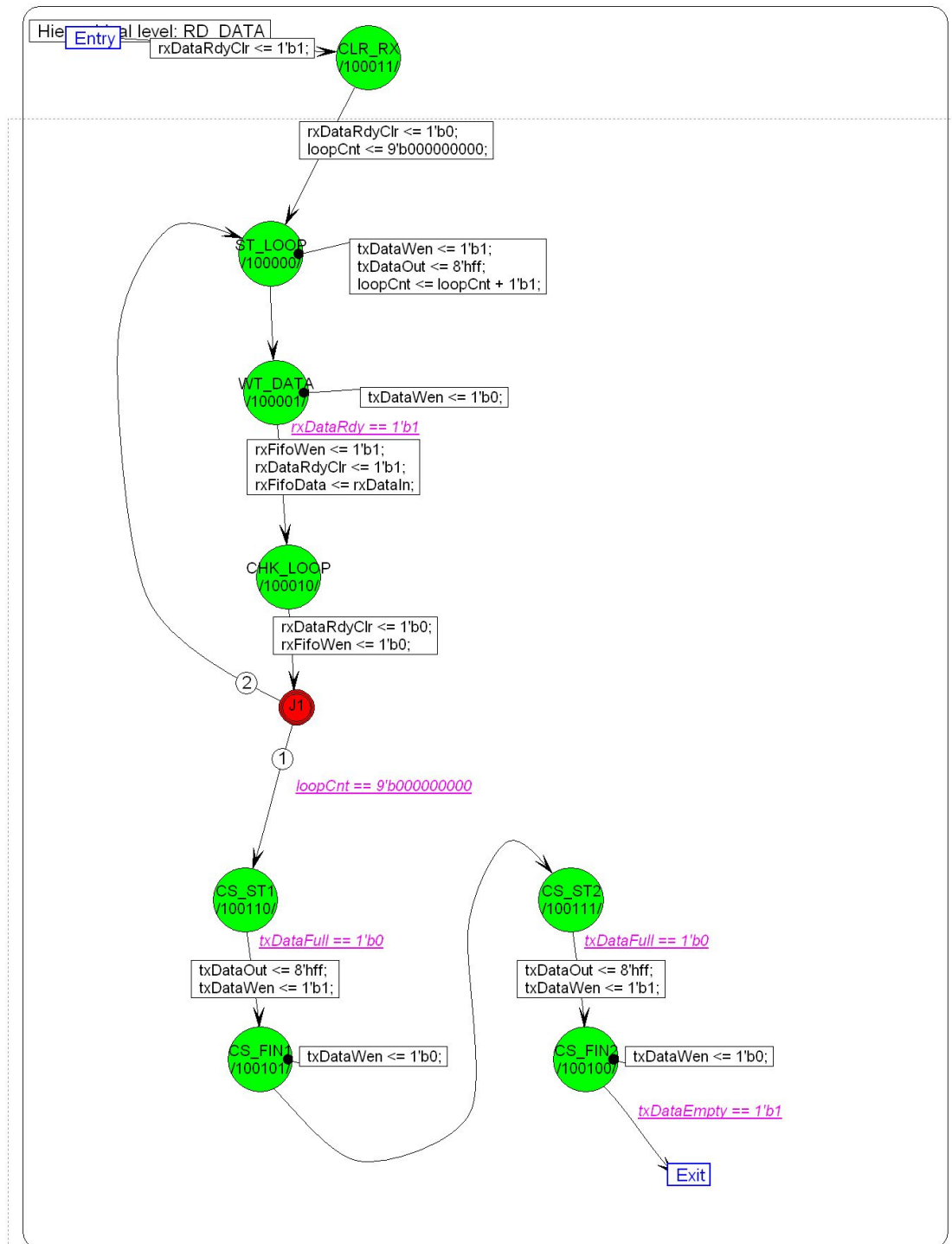
## 2.4.5.1 J2



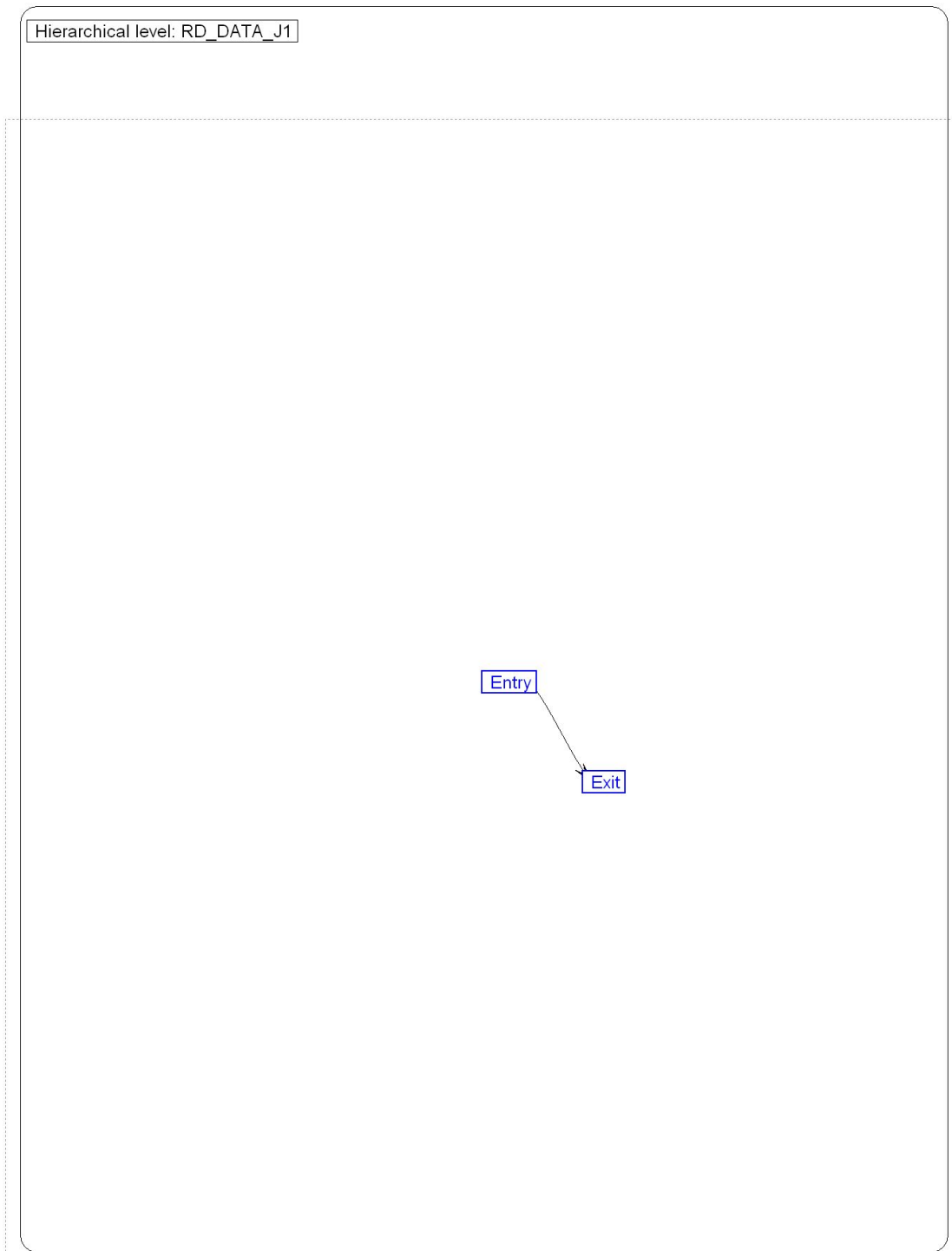
## 2.4.6 RD\_TOKEN



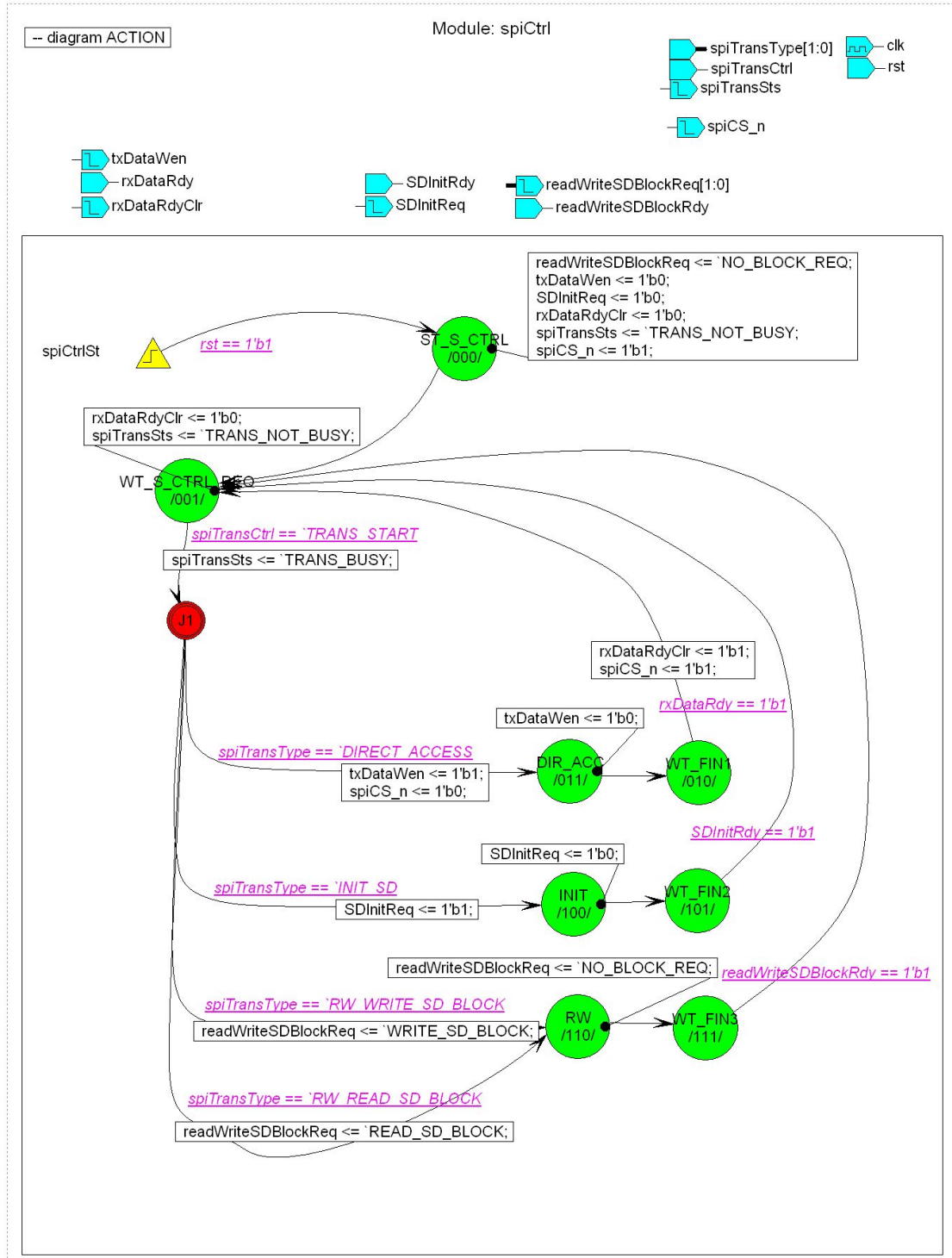
## 2.4.7 RD\_DATA



2.4.7.1 J1



## 2.5 spiCtrl.asf



2.5.1 J1

